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8096 16-Bit Microcontroller Architectural Specification and Functional Description

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8096 16-Bit Microcontroller Architectural Specification and Functional Description

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8096/8396
16-BIT MICROCONTROLLER

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The iACX-96 family of 16-bit microcontrollers consists of the 8096 and the 8396. The 8096 is a 16-bit microcomputer circuit designed for high-speed control functions. The 8396 is an 8096 with 8K bytes of on-chip ROM.

The CPU supports bit, byte, and word operations. 32-bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8096 can do a 16-bit addition in 1.0 μsec and a 16 x 16-bit multiply or 32/16-bit divide in 6.5 μsec Instruction execution times average 1 to 2 μsec in typical applications.

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform timer functions. Up to four such 16-bit Software Timers can be in operation at once.

An optional on-chip A/D Converter converts up to 4 (in the 48-pin version) or 8 (in the 68-pin version) analog input channels to 10-bit digital values.

Also provided on-chip are a serial port, a watchdog timer, and a pulse-width modulated output signal.

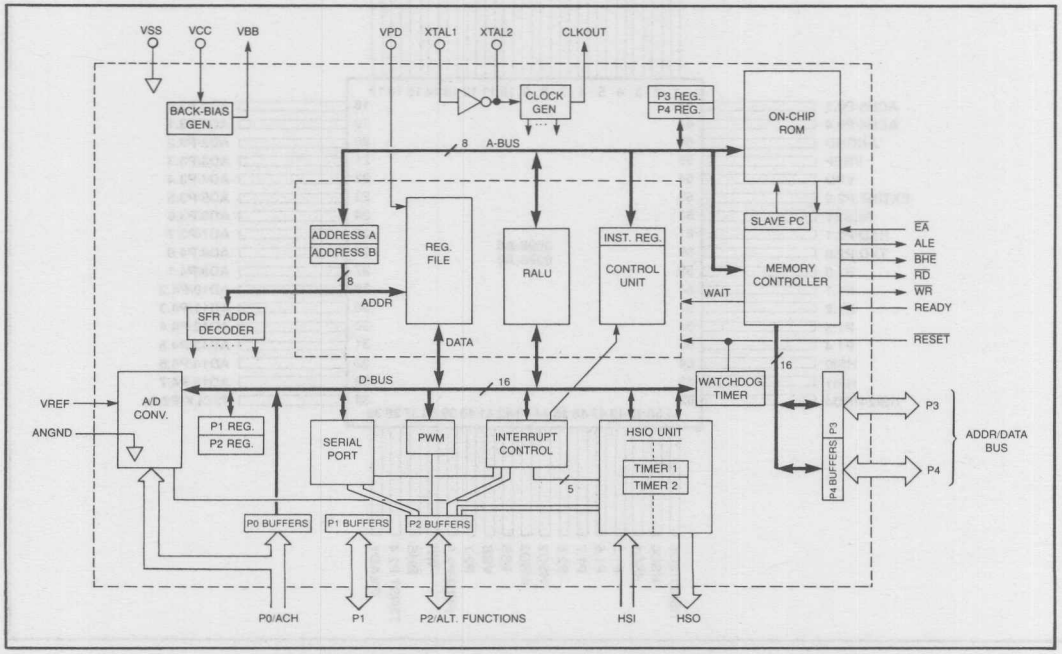

Figure 1. Block Diagram (For simplicity, lines connecting port registers to port buffers are not shown.)

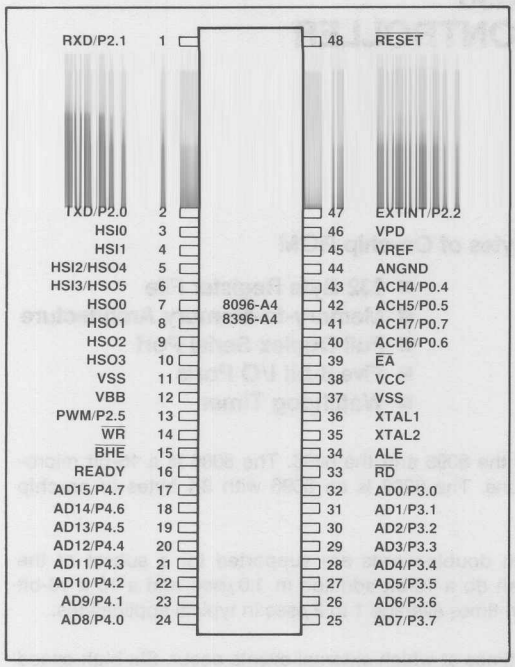

Figure 2. 48-Pin Package

Figure 1 shows the block diagram of the 8396. The 8096 differs only in not having on-chip ROM. Both devices are available in both 48-pin and 68-pin versions. Both devices are available with and without the on-chip A/D Converter. The iACX-96 numbering system is as shown below:

48-Pin	68-Pin	Features	
8096-D4	8096-D6	ROMless	No A/D
8096-A4	8096-A6	ROMless	With A/D
8396-D4	8396-D6	8K-Byte ROM	No A/D
8396-A4	8396-A6	8K-Byte ROM	With A/D

Figures 2 and 3 show the pinouts for the 48- and 68-pin packages.

The microcomputer is organized internally in a double bus structure. Internal data transfers are handled by a 16-bit data bus (D Bus) and an 8-bit address bus (A Bus). The internal registers occupy addresses 0000H through 00FFH. Communication with memory locations above

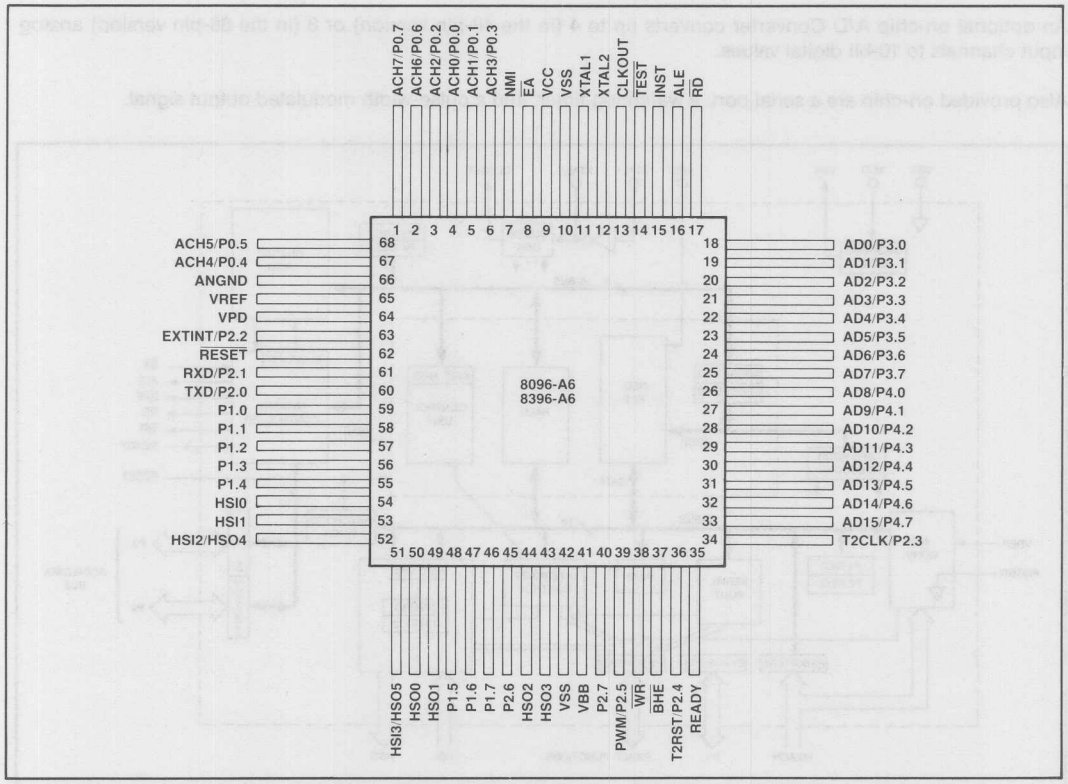

Figure 3. 68-Pin Package

00FFH is through the 8-bit bus and the Memory Controller. Thus the A Bus also conducts instruction and data bytes.

MEMORY SPACE

The 8096 uses the same address space for both program and data memory. It can execute instructions from any memory address. (Instructions cannot, however, be fetched from internal RAM. Instruction fetches from locations 0000H through 00FFH are automatically directed to external memory. These locations in external memory should be reserved for future Intel developments.)

Internal locations 0000H through 0017H are Special Function Registers (ports, control registers, etc.). Locations 0018H through 00FFH access the Register File, of which the top 16 bytes (addresses 00F0H through 00FFH) are preserved during power down if a backup

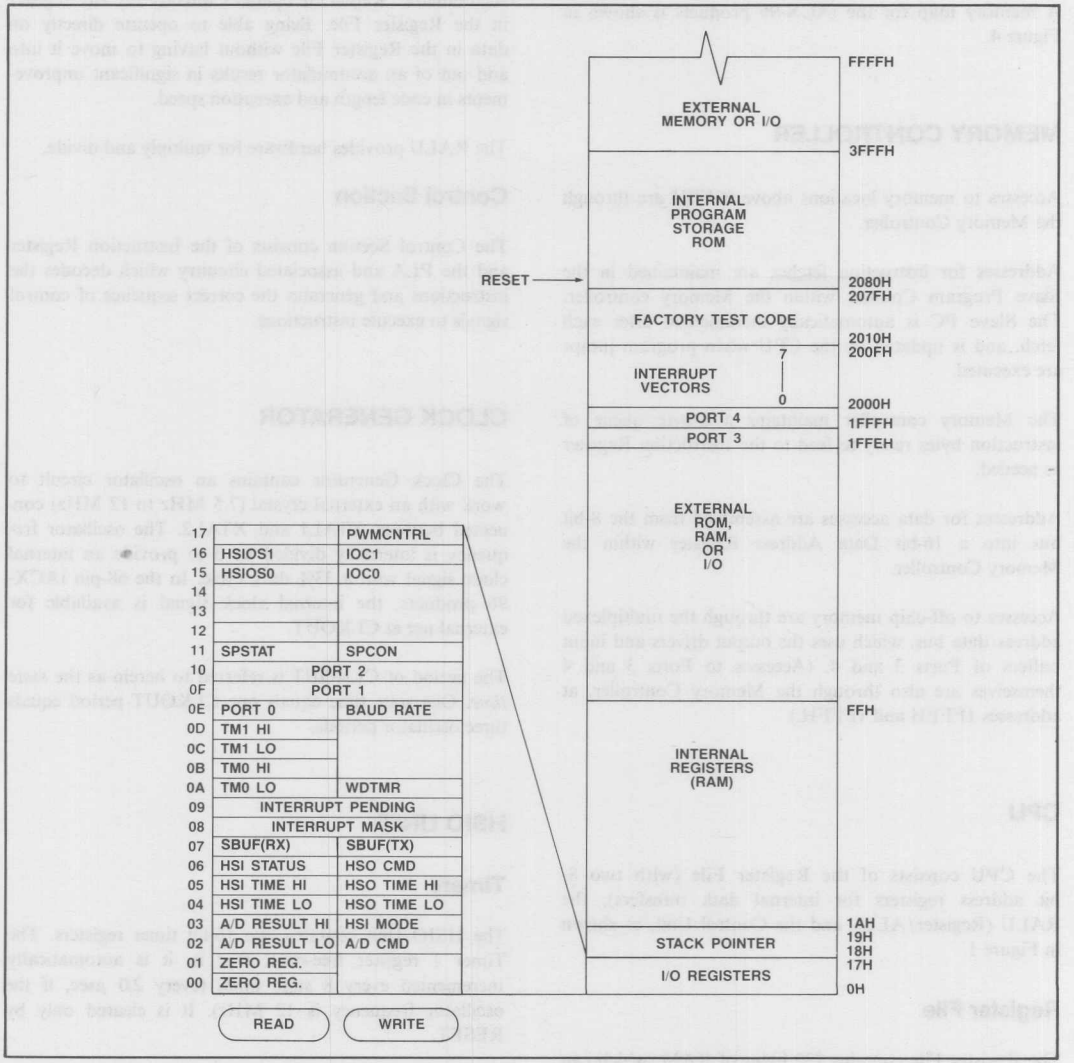

Figure 4. Memory Map

supply is applied to the VPD pin. Locations 0018H and 0019H contain the Stack Pointer.

The 8396 carries 8K bytes of on-chip ROM, occupying addresses 2000H through 3FFFH. These addresses access the on-chip ROM if the $\overline{EA}$ pin is externally held at a logical 1. Otherwise, the same addresses access off-chip memory. Addresses 2000H through 200FH contain the interrupt vectors. Addresses 2010H through 207FH contain a factory test code. Reset commences execution from location 2080H.

A memory map for the iACX-96 products is shown in Figure 4.

MEMORY CONTROLLER

Accesses to memory locations above 00FFH are through the Memory Controller.

Addresses for instruction fetches are maintained in the Slave Program Counter within the Memory controller. The Slave PC is automatically incremented after each fetch, and is updated by the CPU when program jumps are executed.

The Memory controller maintains a 3-byte queue of instruction bytes ready to feed to the Instruction Register as needed.

Addresses for data accesses are assembled from the 8-bit bus into a 16-bit Data Address Register within the Memory Controller.

Accesses to off-chip memory are through the multiplexed address/data bus, which uses the output drivers and input buffers of Ports 3 and 4. (Accesses to Ports 3 and 4 themselves are also through the Memory Controller, at addresses 1FFEH and 1FFFH.)

CPU

The CPU consists of the Register File (with two 8-bit address registers for internal data transfers), the RALU (Register/ALU), and the Control Unit, as shown in Figure 1.

Register File

The Register File contains 232 bytes of RAM, which can be referenced as bytes, words, or double-words. This register space allows the user to keep the most frequently-used variables in on-chip RAM, which can be accessed more quickly than external memory.

RALU

The RALU (Register/ALU) section consists of a 17-bit ALU, the Program Status Word, the Program Counter, and several temporary registers, as shown in Figure 5.

A key feature of the 8096 is that it does not use an accumulator. Rather, it operates directly on any register in the Register File. Being able to operate directly on data in the Register File without having to move it into and out of an accumulator results in significant improvements in code length and execution speed.

The RALU provides hardware for multiply and divide.

Control Section

The Control Section consists of the Instruction Register and the PLA and associated circuitry which decodes the instructions and generates the correct sequence of control signals to execute instructions.

CLOCK GENERATOR

The Clock Generator contains an oscillator circuit to work with an external crystal (7.5 MHz to 12 MHz) connected between XTAL1 and XTAL2. The oscillator frequency is internally divided by 3 to provide an internal clock signal with a 33% duty cycle. In the 68-pin iACX-96 products, the internal clock signal is available for external use at CLKOUT.

The period of CLKOUT is referred to herein as the *state time*. One state time equals one CLKOUT period equals three oscillator periods.

HSIO UNIT

Timers

The HSIO Unit contains two 16-bit timer registers. The Timer 1 register free-runs, that is, it is automatically incremented every 8 state times (every 2.0 μsec, if the oscillator frequency is 12 MHz). It is cleared only by RESET.

The Timer 2 register, also 16 bits, can be programmed to

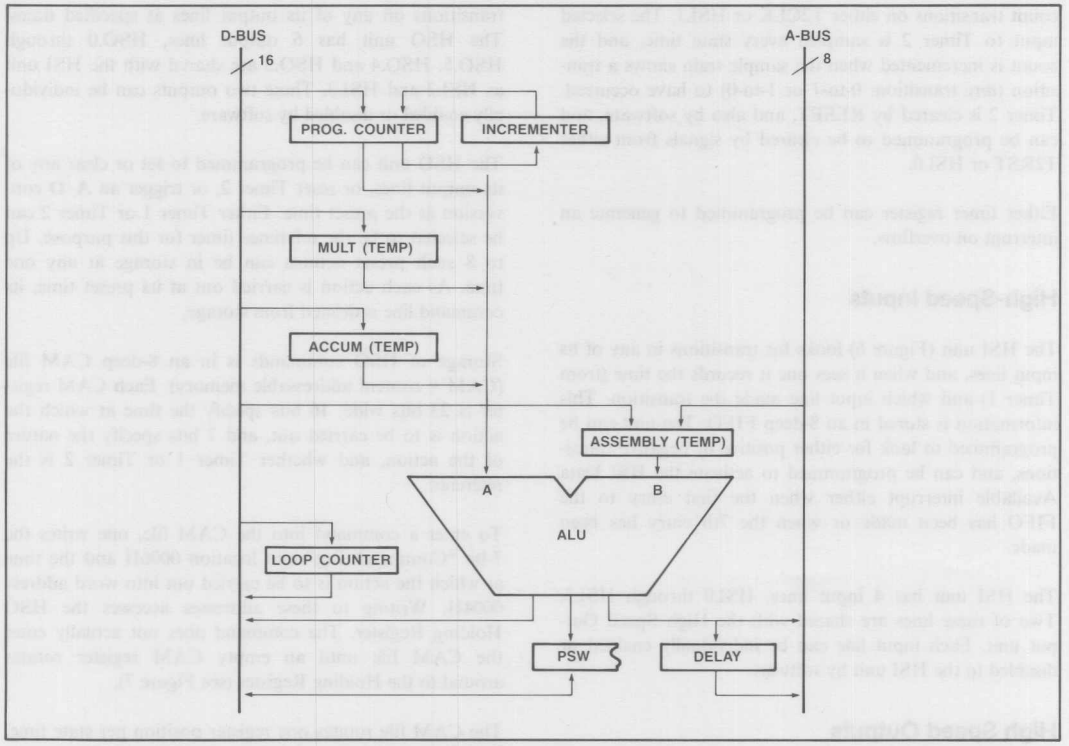

Figure 5. RALU

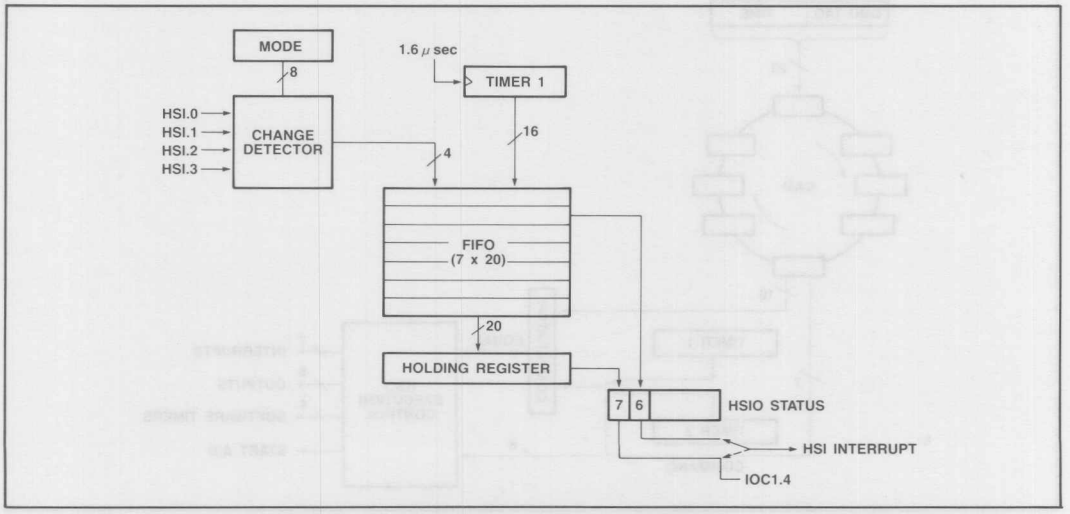

Figure 6. HSI Unit

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count transitions on either T2CLK or HSI.1. The selected input to Timer 2 is sampled every state time, and the count is incremented when the sample train shows a transition (*any* transition: 0-to-1 or 1-to-0) to have occurred. Timer 2 is cleared by RESET, and also by software, and can be programmed to be cleared by signals from either T2RST or HSI.0.

Either timer register can be programmed to generate an interrupt on overflow.

High-Speed Inputs

The HSI unit (Figure 6) looks for transitions in any of its input lines, and when it sees one it records the time (from Timer 1) and which input line made the transition. This information is stored in an 8-deep FIFO. The unit can be programmed to look for either positive or negative transitions, and can be programmed to activate the HSI Data Available interrupt either when the first entry to the FIFO has been made or when the 7th entry has been made.

The HSI unit has 4 input lines, HSI.0 through HSI.3. Two of these lines are shared with the High Speed Output unit. Each input line can be individually enabled or disabled to the HSI unit by software.

High Speed Outputs

The HSO unit (Figure 7) can be programmed to cause transitions on any of its output lines at specified times. The HSO unit has 6 output lines, HSO.0 through HSO.5. HSO.4 and HSO.5 are shared with the HSI unit as HSI.2 and HSI.3. These two outputs can be individually enabled or disabled by software.

The HSO unit can be programmed to set or clear any of its output lines, or reset Timer 2, or trigger an A/D conversion at the preset time. Either Timer 1 or Timer 2 can be selected to be the reference timer for this purpose. Up to 8 such preset actions can be in storage at any one time. As each action is carried out at its preset time, its command line is deleted from storage.

Storage of HSO commands is in an 8-deep CAM file (CAM = content addressable memory). Each CAM register is 23 bits wide. 16 bits specify the time at which the action is to be carried out, and 7 bits specify the nature of the action, and whether Timer 1 or Timer 2 is the reference.

To enter a command into the CAM file, one writes the 7-bit "Command Tag" into location 0006H and the time at which the action is to be carried out into word address 0004H. Writing to these addresses accesses the HSO Holding Register. The command does not actually enter the CAM file until an empty CAM register rotates around to the Holding Register (see Figure 7).

The CAM file rotates one register position per state time. Thus it takes 8 state times for the Holding Register to have had access to all 8 CAM registers. Similarly, it takes

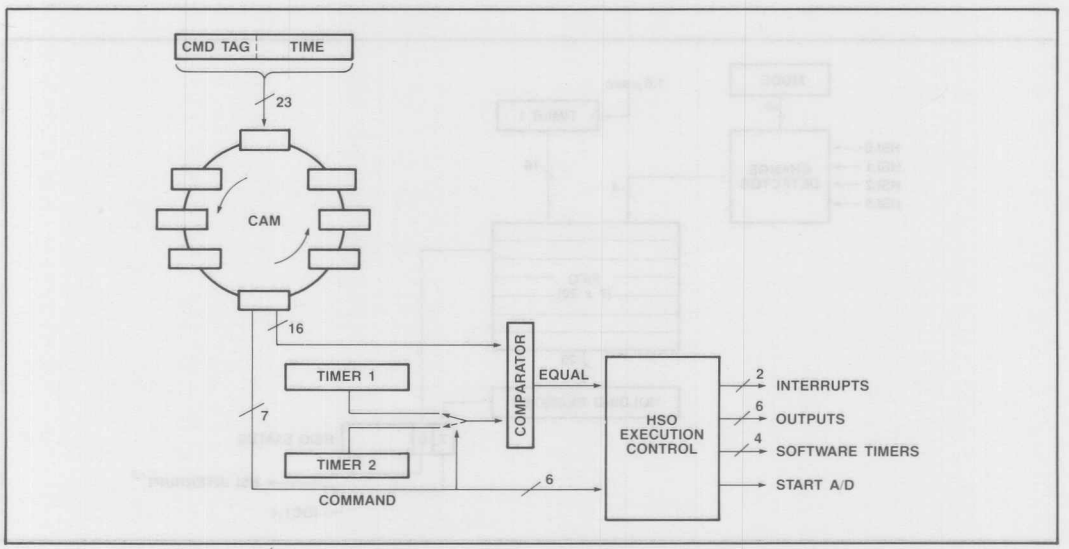


Figure 7. HSO Unit

8 state times for the comparator to have had access to all 8 CAM registers. This defines the time-resolution of the HSO unit to be 8 state times (2.0 μsec, if the oscillator frequency is 12 MHz).

Timer 1 is incremented only once every 8 state times, so if Timer 1 is being used as the reference timer for an HSO action, the comparator has a chance to look at all 8 CAM registers before Timer 1 changes its value. If Timer 2 is being used as the reference timer, the user must ensure that it does not increment more often than once every 8 state times, lest a target-time for an HSO action come and go before that particular command line rotates around to the comparator.

Software Timers

The HSO can be programmed to generate interrupts at preset times. Up to four such "Software Timers" can be in operation at a time. As each preset time is reached, the HSO unit generates a Software Timer interrupt. The interrupt service routine can then examine an HSIO status register (HSIOS1) to determine which software timer expired and caused the interrupt.

The effect is essentially the same as having four additional 16-bit timers.

I/O PORTS

Input ports connect to the internal bus through an input buffer. Output ports connect through an output buffer to an internal register that holds the output bits. Bidirectional ports consist of an internal register, an output buffer, and an input buffer. Bidirectional ports are shown in Figure 1 as consisting of two separate blocks: the internal register and the I/O buffer.

When an instruction accesses a bidirectional port as a source register, the question often arises as to whether the value that is brought into the CPU comes from the internal port register or from the port pins through the input buffer. In the 8096, the value always comes from the port pins, never from the internal register.

Port 0 is an input-only port which shares its pins with the analog inputs to the A/D Converter. One can read Port 0 digitally and/or, by writing the appropriate control bits to the A/D Command Register, select one of the lines of this port to be the input to the A/D Converter.

Port 1 is a quasi-bidirectional I/O port. "Quasi-bidirectional" means the port pin has a weak internal pullup that is always active and an internal pulldown which can either be on (to output a 0) or off (to output a 1). If the internal pulldown is left off (by writing a 1 to the pin), the pin's logic level can be controlled by an external pulldown which can either be on (to input a 0) or off (to input a 1). From the user's point of view the main distinction is that a quasi-bidirectional input will source current while being externally held low.

In parallel with the weak internal pullup is a much stronger internal pullup that is activated for one state time when the pin is internally driven from 0 to 1. This is done to speed up the 0-to-1 transition time.

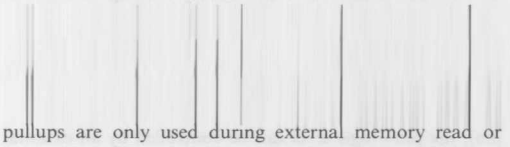
Port 2 is a multi-functional port. Six of its pins are shared with other functions in the 8096, as shown below:

Port Function		Alternate Function
P2.0	output	TXD (serial port transmit)
P2.1	input	RXD (serial port receive)
P2.2	input	EXTINT (external interrupt)
P2.3	input	T2CLK (Timer 2 input)
P2.4	input	T2RST (Timer 2 reset)
P2.5	output	PWM (pulse-width modulated signal)
P2.6	quasi-bidirectional	
P2.7	quasi-bidirectional	

Ports 3 and 4 are bidirectional with open-drain outputs in all pins. Also, these two ports share their pins with the Memory Controller, as shown below:

Port Pin	System Bus Function
P3.0	AD0
P3.1	AD1
P3.2	AD2
P3.3	AD3
P3.4	AD4
P3.5	AD5
P3.6	AD6
P3.7	AD7
P4.0	AD8
P4.1	AD9
P4.2	AD10
P4.3	AD11
P4.4	AD12
P4.5	AD13
P4.6	AD14
P4.7	AD15

When these pins are being used by the Memory Controller, they do have strong internal pullups. The internal



pullups are only used during external memory read or write cycles when the pins are outputting address or data bits. At any other time, the internal pullups are disabled.

SERIAL PORT

The serial port is compatible with the MCS-51 serial port. It is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. The serial port registers are both accessed at the same address. A write to this location accesses the transmit register, and a read accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Mode 0 is a shift register mode. The 8096 outputs a train of 8 shift pulses to an external shift register to clock 8 bits of data into or out of the register from or to the 8096. Serial data enters and exits the 8096 through RXD. TXD outputs the shift signal. 8 bits are transmitted or received, LSB first. This mode is useful as an I/O expander, in which application external shift registers can be used as additional parallel I/O ports.

Mode 1: 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1).

Mode 2: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit can be assigned the value of 0 or 1. On receive, the serial port interrupt is not activated unless the received 9th data bit is 1.

Mode 3: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit can be assigned the value of 0 or 1. On receive, the received 9th data bit is stored, and the serial port interrupt is activated regardless of its value.

Mode 2 is provided for multi-processor communications. In this mode if the received 9th data bit is not 1, the serial port interrupt is not activated. The way to use this feature in multi-processor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address frame which identifies the target slave. An address frame will differ from a data frame in that the 9th data bit is 1 in an address frame and 0 in a data frame. No slave in

mode 2 will be interrupted by a data frame. An address frame, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave switches to mode 3 to receive the coming data frames, while the slaves that weren't addressed stay in mode 2 and go on about their business.

Baud rates in all modes are determined by the contents of a 16-bit register. The MSB of this register selects one of two sources for the input frequency to the baud rate generator: the oscillator frequency or an external frequency from the T2CLK pin. The unsigned integer represented by the remaining 15 bits of the baud rate register, plus 1, defines a number B, where B can thus take any value from 1 to 32768. The baud rate for the 4 serial modes is then given by

Mode 0: baud rate = input frequency/(4*B)

Others: baud rate = input frequency/(64*B)

PULSE WIDTH MODULATOR

The PWM output shares a pin with port bit P2.5. A bit in control register IOC1 selects the function of this pin to be either PWM or P2.5. When PWM is selected, this pin outputs a pulse train having a fixed period of 256 state times, and a programmable width of 0 to 255 state times. The width is programmed by loading the desired value, in state times, to the PWM Control Register.

A/D CONVERTER

The analog-to-digital converter is a 10-bit, successive approximation converter. This type of converter has a fixed conversion time, in this case 168 state times, independent of the value of the analog input. The analog input must be in the range of 0 to VREF (normally, VREF = 5V). This input can be selected from 8 analog input lines, which connect to the same pins as Port 0. A conversion can be initiated either by setting a control bit in the A/D Command register, or by programming the HSO unit to trigger the conversion at some specified time.

INTERRUPTS

The interrupt structure for the 8096 is shown in Figure 8.

The 8096 has 8 interrupt sources. A 0-to-1 transition from any of the sources sets a corresponding bit in the Interrupt Pending register. The content of the Interrupt Mask register determines if a pending interrupt will be responded to or not. If it is to be responded to, the CPU pushes the current Program Counter onto the Stack and reloads it with the vector corresponding to the interrupt being responded to. The interrupt vectors are located in addresses 2000H through 200FH, as shown below:

Interrupt Source	Vector Location	
	high byte	*low byte*
EXTINT	200FH	200EH
Serial Port	200DH	200CH
Software Timers	200BH	200AH
HSI.0	2009H	2008H
High Speed Outputs	2007H	2006H
HSI Data Available	2005H	2004H
A/D Conversion Complete	2003H	2002H
Timer Overflow	2001H	2000H

Execution then vectors to the ISR (interrupt service routine). At least one instruction in the ISR will always be executed before a second interrupt can be responded to. Any ISR can itself be interrupted, but not before the first instruction of the current ISR has been executed. Normally, this first instruction is PUSHF (push flags). PUSHF does two things: First it pushes the current PSW onto the Stack, and then it clears the PSW. Clearing the PSW clears the Interrupt Mask register, in effect blocking further interrupts. In the next instruction, if the programmer so desires, interrupts from selected sources can be re-enabled. In this manner, the software determines the priority structure.

The ISR then would normally terminate with POPF (pop flags), which restores the original PSW, and RET, which

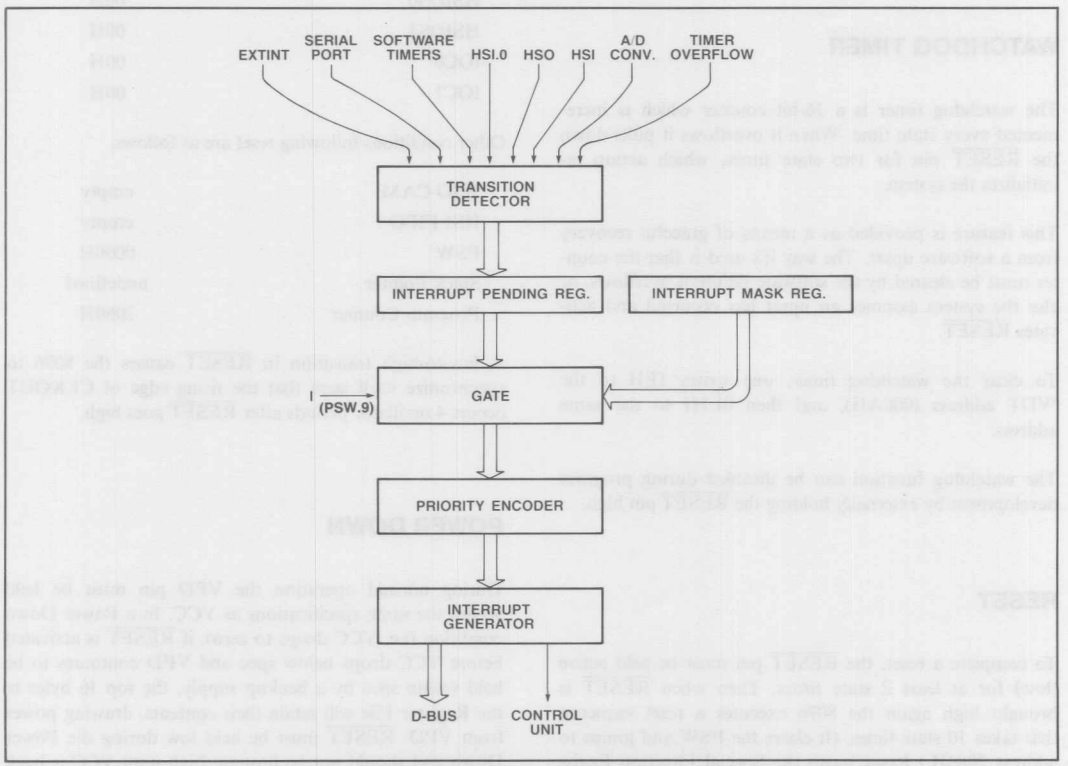
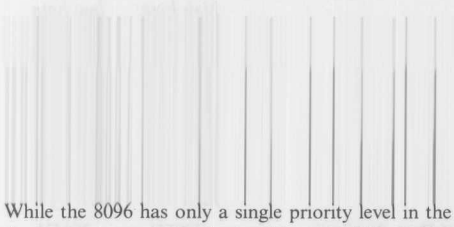


Figure 8. Interrupt Structure

restores the original Program Counter.



While the 8096 has only a single priority level in the sense that any interrupt may be itself interruptible, it does have a priority structure for resolving *simultaneous* interrupts, as follows:

Source	Priority
EXTINT	7 (highest)
Serial Port	6
Software Timers	5
HSI.0	4
High Speed Outputs	3
HSI Data Available	2
A/D Conversion Complete	1
Timer Overflow	0 (lowest)

WATCHDOG TIMER

The watchdog timer is a 16-bit counter which is incremented every state time. When it overflows it pulls down the $\overline{\text{RESET}}$ pin for two state times, which action reinitializes the system.

This feature is provided as a means of graceful recovery from a software upset. The way it's used is that the counter must be cleared by the software before it overflows, or else the system assumes an upset has occurred and activates $\overline{\text{RESET}}$.

To clear the watchdog timer, one writes 1EH to the WDT address (000AH), and then 0E1H to the same address.

The watchdog function can be disabled during program development by externally holding the $\overline{\text{RESET}}$ pin high.

RESET

To complete a reset, the $\overline{\text{RESET}}$ pin must be held active (low) for at least 2 state times. Then when $\overline{\text{RESET}}$ is brought high again the 8096 executes a reset sequence that takes 10 state times. (It clears the PSW and jumps to address 2080H.) Reset leaves the Special Function Registers as follows:

SFR	Reset Value
Port 1	0FFH
Port 2	11XXXXX1B
Port 3	0FFH
Port 4	0FFH
PWM Control	00H
Serial Port (Transmit)	undefined
Serial Port (Receive)	undefined
Baud Rate Register	undefined
Serial Control/Status	undefined
A/D Command	undefined
A/D Result	undefined
Interrupt Pending	undefined
Interrupt Mask	00H
Timer 1	0000H
Timer 2	0000H
Watchdog Timer	0000H
HSI Mode	00H
HSI Status	undefined
HSIOS0	00H
HSIOS1	00H
IOC0	00H
IOC1	00H

Other conditions following reset are as follows:

HSO CAM	empty
HSI FIFO	empty
PSW	0000H
Stack Pointer	undefined
Program Counter	2080H

A low-to-high transition in $\overline{\text{RESET}}$ causes the 8096 to synchronize itself such that the rising edge of CLKOUT occurs 4 oscillator periods after $\overline{\text{RESET}}$ goes high.

POWER DOWN

During normal operation the VPD pin must be held within the same specifications as VCC. In a Power Down condition (i.e. VCC drops to zero), if $\overline{\text{RESET}}$ is activated before VCC drops below spec and VPD continues to be held within spec by a backup supply, the top 16 bytes in the Register File will retain their contents, drawing power from VPD. $\overline{\text{RESET}}$ must be held low during the Power Down and should not be brought high until VCC is back and the oscillator has stabilized.

SPECIAL FUNCTION REGISTERS

PWM Control Register

The width of the PWM output pulse is programmed by writing the desired value, in state times (0 to 0FFH) into this register.

Serial Port Control/Status Register

Bit:	7	6	5	4	3	2	1	0
	RB8/RPE	RI	TI	TB8	REN	PEN	M2	M1

where: M1,M2 specifies the Mode;
PEN enables the parity function (even parity);
REN enables the receive function;
TB8 programs the 9th data bit (if not parity) on transmission;
TI is the transmit interrupt flag;
RI is the receive interrupt flag;
RB8 is the 9th data bit received (if not parity);
RPE is the parity error indicator (if parity active).

A/D Command Register

Bit:	7	6	5	4	3	2	1	0
	X	X	X	X	GO	.... channel #		

where: channel # selects which of the 8 analog input channels is to be converted to digital form;
GO indicates when the conversion is to be initiated (GO = 1 means start now, GO = 0 means the conversion is to be initiated by the HSO unit at a specified time).

A/D Result Register

Bit:	15	6	5	4	3	2	1	0
	MSB.....LSB	X	X	S	... channel # ...			
	(10-bit A/D Result)							

where: channel # tells which of the 8 analog input channels this was converted from;
S is a STATUS bit (S = 1 means an A/D conversion is currently under way, S = 0 means the A/D unit is currently idle).

Because of the way the A/D Result Register is implemented on the chip, it must be read as two separate bytes.

Interrupt Registers

The Interrupt Pending and Mask Registers each contain one bit for each of the 8 interrupt sources: Bit 7 is for the highest priority source (EXTINT) and bit 0 is for the lowest priority source (Timer Overflow). The Interrupt Mask Register is the low byte of the PSW.

HSI Mode Register

As previously described, the HSI unit looks for transitions of a desired type in its input lines, and when it sees one it records the time (from Timer 1) and in which input line the transition occurred.

The HSI Mode register defines what kinds of input transitions cause the contents of Timer 1 to be captured into the HSI FIFO, as follows:

Bit:	7	6	5	4	3	2	1	0
	/ HSI.3 Mode		/ HSI.2 Mode		/ HSI.1 Mode		/ HSI.0 Mode	/

Each 2-bit mode control field defines one of 4 possible modes:

0 0	8 positive transitions
0 1	positive transitions
1 0	negative transitions
1 1	any transition

High and low levels need to hold for at least 1 state time or they may be missed.

HSI Status Register

The HSI Status register tells which input made a targeted transition and what its current state is (0 or 1), as follows:

Bit:	7	6	5	4	3	2	1	0
	/ HSI.3	/	HSI.2	/	HSI.1	/	HSI.0	/

For each 2-bit field, the lower bit indicates whether or not the transition has been made at this input, and the upper bit gives the current state at that pin.

HSO Command Tag

The HSO unit can be programmed to cause transitions in any of its output lines at specified times. The specified time can be taken from either Timer 1 or Timer 2. The unit has 6 output lines, but 2 of them (HSO.4 and

HSO.5) are shared by the HSI unit. The unit can initiate a number of other actions at specified times: initiate an A/D conversion, reset Timer 2, or indicate a software timer timeout. It can initiate these actions with or without an accompanying interrupt.

The HSO Command register is as follows:

Bit:	7	6	5	4	3	2	1	0
	X	T	1/0	I	. . . . .	channel #	. . . . .	

where: channel # defines the recipient of the action;
I says whether or not the action is to be accompanied by an interrupt;
1/0 says whether the action on an output line is to be set to 1 or to 0;
T selects whether the "specified time" is to be from Timer 1 (T = 0) or Timer 2 (T = 1).

The channel # codes are as follows:

Channel #	Recipient of Action
0–5H	Output lines HSO.0–HSO.5
6H	Output lines HSO.0 and HSO.1 combined
7H	Output lines HSO.2 and HSO.3 combined
8H–0BH	Software Timers ST0–ST3 (the action being to establish it)
0EH	Timer 2 (the action being to reset it)
0FH	A/D Converter (the action being to initiate a conversion)

I/O Control Registers

There are two I/O Control registers, IOC0 and IOC1. IOC0 conditions Timer 2 and the HSI lines. IOC1 selects some pin functions and enables or disables some interrupt sources.

Timer 2 can count one of two selectable clock sources, T2CLK or HSI.1. It can be reset by one of two selectable hardware sources (T2RST or HSI.0) or by timed software (through the HSO unit) or by immediate software (through IOC0 bit 1). The selected hardware reset source pin can be enabled or disabled to this function.

The four HSI lines can be enabled or disabled to the HSI unit by setting or clearing bits in IOC0.

The bits of IOC0 are as follows:

Bit	Control Function
0	Set to 1 to enable HSI.0 to the HSI function. Clear to 0 to disable HSI.0 to the HSI function. (It can still be used to reset Timer 2, however.)
1	Writing a 1 to this bit resets Timer 2 every time.
2	Set to 1 to enable HSI.1 to the HSI function. Clear to 0 to disable HSI.1 to the HSI function. (It can still be used to clock Timer 2, however.)
3	Set to 1 to enable the external Timer 2 reset source (T2RST or HSI.0). Clear to disable same.
4	Set to 1 to enable HSI.2 to the HSI function.
5	Select external Timer 2 reset source: 0 selects T2RST; 1 selects HSI.0.
6	Set to 1 to enable HSI.3 to the HSI function.
7	Select Timer 2 clock source: 0 selects T2CLK; 1 selects HSI.1

IOC1 selects some pin functions and enables or disables some interrupt sources. Port pin P2.5 can be selected to be the PWM output. The external interrupt source can be selected to be either EXTINT (same pin as P2.2) or Analog Channel 7 (ACH7, same pin as P0.7). Timer 1 and Timer 2 overflow interrupts can be individually enabled or disabled. The HSI interrupt can be selected to activate either when there is 1 FIFO entry or 7. Port pin P2.0 can be selected to be the TXD output. HSO.4 and HSO.5 can be enabled or disabled to the HSO unit.

The bits of IOC1 are as follows:

Bit	Control Function
0	Select pin function: If this bit is 1, P2.5 becomes PWM.
1	Select external interrupt source: 0 selects EXTINT; 1 selects ACH7 (P0.7).
2	Set to 1 to enable Timer 1 overflow interrupt. Clear to disable same.
3	Set to 1 to enable Timer 2 overflow interrupt. Clear to disable same.
4	HSI interrupt option: 0 selects to activate interrupt at first entry to FIFO. 1 selects to activate on 7th entry
5	Select pin function: If this bit is 1, P2.0 becomes TXD.
6	Set to 1 to enable HSO.4 to the HSO function.
7	Set to 1 to enable HSO.5 to the HSO function.

HSIO Status Registers

There are two HSIO Status registers. One gives the current status of the HSO lines and CAM. The other gives the overflow status of the 4 software timers, and of Timers 1 and 2, and indicates the status of the HSI FIFO.

The bits of HSIOS0 are as follows:

Bit	Function
0	Current state of HSO.0
1	Current state of HSO.1
2	Current state of HSO.2
3	Current state of HSO.3
4	Current state of HSO.4
5	Current state of HSO.5
6	A 0 indicates that the HSO Holding Register is empty and there is at least one empty register in the CAM.
7	A 0 indicates that the HSO Holding Register is empty.

The bits of HSIOS1 are as follows:

Bit	Function
0	A value 1 indicates Software Timer 0 has expired.
1	A value 1 indicates Software Timer 1 has expired.
2	A value 1 indicates Software Timer 2 has expired.
3	A value 1 indicates Software Timer 3 has expired.
4	A value 1 indicates Timer 2 has overflowed.
5	A value 1 indicates Timer 1 has overflowed.
6	A value 1 indicates the HSI FIFO contains at least seven entries.
7	A value 1 indicates the HSI FIFO contains at least one entry.

PIN DESCRIPTION

VCC

Main supply voltage (5V).

VSS

Digital circuit ground (0V).

VPD

RAM standby supply voltage (5V). This voltage must be present during normal operation.

VREF

Reference voltage for the A/D converter (5V). VREF is also the supply voltage to the analog portion of the A/D converter.

ANGND

Reference ground for the A/D converter. Should be held at nominally the same potential as VSS.

VBB

Substrate voltage from the on-chip back-bias generator. This pin should be connected to ANGND through a 0.01 μf capacitor (and not connected to anything else).

XTAL1

Input of the oscillator inverter.

XTAL2

Output of the oscillator inverter, and input to the internal clock generator.

CLKOUT

Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle. CLKOUT can drive one S TTL input.

$\overline{\text{RESET}}$

Reset input to the chip. Input low for at least 2 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared and a jump to address 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has a strong internal pullup.

$\overline{\text{TEST}}$

Input low enables a factory test mode. The user should tie this pin to VCC for normal operation.

NMI

Input high disables internal interrupts and the watchdog timer, and causes a vector to *external* memory location 0000H.

INST

Output high during an external memory read indicates the read is an instruction fetch.

$\overline{EA}$

Input for memory select (External Access). $\overline{EA}$ = 1 causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM. $\overline{EA}$ = 0 causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ has an internal pulldown, so it goes to 0 unless driven to 1.

ALE

Address Latch Enable output. ALE is activated only during external memory accesses. It is used to latch the address from the multiplexed address/data bus. ALE can drive one S TTL input.

$\overline{RD}$

Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads. $\overline{RD}$ can drive one S TTL input.

$\overline{WR}$

Write signal output to external memory. $\overline{WR}$ is activated only during external memory writes. $\overline{WR}$ can drive one S TTL input.

$\overline{BHE}$

Bus High Enable signal output to external memory. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit-wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0), or to both bytes (A0 = 0, $\overline{BHE}$ = 0). $\overline{BHE}$ is activated by the Bus Interface Unit when required during accesses to external memory. $\overline{BHE}$ can drive one S TTL input.

READY

The READY input is used to lengthen external memory bus cycles, for interfacing to slow or dynamic memory, or for bus sharing. READY is sampled by the Memory Controller at the negative transition in CLKOUT while $\overline{RD}$ or $\overline{WR}$ is active during external memory cycles. If the pin is high (READY = 1), CPU operation continues in a normal manner. If the pin is low (READY = 0) when sampled, the Memory Controller goes into a wait mode until the next negative transition in CLKOUT, at which time READY is sampled again. The bus cycle can be lengthened by up to 1 μsec. When the external memory bus is not being used, READY has no effect. READY has a weak internal pullup, so it goes to 1 unless externally pulled down.

HSI

High impedance inputs to HSI Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2, and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.

HSO

Outputs from HSO Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4, and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit. All HSO pins are capable of driving one S TTL input.

Port 0

High impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.

Port 1

Quasi-bidirectional I/O port. All pins of P1 are capable of driving one LS TTL input.

Port 2

Multi-functional port. Six of its pins are shared with other functions in the 8096, as shown below:

Port Function		Alternate Function
P2.0	output	TXD (serial port transmit)
P2.1	input	RXD (serial port receive)
P2.2	input	EXTINT (external interrupt)
P2.3	input	T2CLK (Timer 2 input)

Port Function		Alternate Function
P2.4	input	T2RST (Timer 2 reset)
P2.5	output	PWM (pulse-width modulated signal)
P2.6	quasi-bidirectional	
P2.7	quasi-bidirectional	

The quasi-bidirectional pins can drive one LS TTL input. The multi-functional outputs can drive one S TTL input. The multi-functional inputs are high impedance.

Ports 3 and 4

8-bit bidirectional I/O ports with open drain outputs. These pins are also the multiplexed address/data bus when accessing external memory, as shown below:

Port Pin	System Bus Function
P3.0	AD0
P3.1	AD1
P3.2	AD2
P3.3	AD3
P3.4	AD4
P3.5	AD5
P3.6	AD6
P3.7	AD7
P4.0	AD8
P4.1	AD9
P4.2	AD10
P4.3	AD11
P4.4	AD12
P4.5	AD13
P4.6	AD14
P4.7	AD15

When these pins are being used by the Memory Controller, they do have strong internal pullups. The internal pullups are only used during external memory read or write cycles when the pins are outputting address or data bits, in which application they can drive one S TTL input. At any other time, the internal pullups are disabled.

When these pins are being used as output ports, they can drive one LS TTL input. As input ports, they are high impedance.

INSTRUCTION SET

Program Status Word (PSW)

The low byte of the PSW is the Interrupt Mask register. The high byte is as follows:

Bit:	15	14	13	12	11	10	9	8
	Z	N	V	VT	C	(X)	I	ST

- Z — Zero bit. Z = 1 means the result of the previous operation was zero. (ADDC and SUBC can clear Z, but they can't set it.)
- N — Negative bit. N = 1 means the algebraically correct result is negative. (The actual result as stored may have an incorrect sign due to an overflow, but N reflects the algebraically correct sign.)
- V — Overflow bit. V = 1 means the magnitude of the algebraically correct result is too large to be correctly represented in the available space.
- VT — Overflow Trap bit. Any time V gets set, VT gets set too. Subsequent operations may clear V, but VT can only be cleared by software.
- C — Carry bit. This is the carry out of the MSB of the result of any arithmetic operation. During left-shifts, the MSB moves into C and a 0 moves into the LSB. During right-shifts, the LSB moves into C and a 0 moves into the MSB.
- (X) — Unused. (Reads 0.)
- I — Interrupt enable bit. I = 0 disables all interrupts.
- ST — Sticky Bit. During right-shifts the LSB moves into C. If the previous value of C was 1, ST gets set (see SHR and SHRA instructions.).

Word Operations

B and D must be located in the Register File. A can be located anywhere in memory.

In the following descriptions, the symbols A, B, and D represent word operands except where noted. Word addresses must be even numbers.

A and B are source registers. D is the destination register.

ARITHMETIC WORD OPERATIONS

Mnemonic	*Meaning*	*Operation*	*Explanation/Rules*
ADD	Add 2 words.	D = D + A D = B + A	
ADDC	Add with carry.	D = D + A + C	C is the carry bit.
SUB	Subtract one word from another.	D = D – A D = B – A	
SUBC	Subtract with carry.	D = D – A – 1 + C	C is the carry bit.
MUL	Multiply 2 words to form a double-word product.	D, D + 2 = D*A D, D + 2 = B*A	The address of the product must be a legal double-word address; that is, it must be evenly divisible by 4.
MULU	Multiplying unsigned.	D, D + 2 = D*A D, D + 2 = B*A	Same as MUL, except operands are treated as unsigned integers.
DIV	Divide a double-word integer by a single-word integer.	D = (D, D + 2) / A D + 2 = remainder	The address of D must be a valid double-word address; that is, it must be evenly divisible by 4.
DIVU	Divide unsigned.	D = (D, D + 2) / A D + 2 = remainder	Same as DIV, except operands are treated as unsigned integers.
INC	Increment word.	D = D + 1	
DEC	Decrement word.	D = D – 1	
CMP	Compare two words.	B – A	The result of the subtraction (B – A) is not stored. Only the PSW is affected.
NEG	Negate word.	D = – D	Changes the sign of the addressed word.
EXTB	Extend byte to word.	D = D D + 1 = SIGN(D)	Sign-extends the addressed byte to word-length. (Hence the address of D must be a valid word-address.)
EXT	Extend word to double-word.	D = D D + 2 = SIGN(D)	Sign-extends the addressed word to double-word length. (Hence the address of D must be a valid double-word address.)

LOGICAL WORD OPERATIONS

Mnemonic	*Meaning*	*Operation*
AND	Logical AND.	D = D AND A D = B AND A
OR	Logical OR.	D = D OR A
XOR	Exclusive OR.	D = D XOR A
NOT	Logical NOT.	D = NOT(D)
CLR	Clear word.	D = 0000H

DATA TRANSFER

Mnemonic	*Meaning*	*Operation*	*Explanation/ Rules*
LD	Load word.	D = A	Both operands are words.
ST	Store word.	A = B	Both operands are words. B must be in the Register File. In this case A, which can be anywhere in memory, is the destination register.
LDBSE	Load byte sign-extended to word.	D = A D + 1 = SIGN(A)	D is a word. A is a byte.
LDBZE	Load byte zero-extended to word.	D = A D + 1 = 00H	D is a word. A is a byte.
PUSH	Push word.	SP = SP – 2 (SP) = A	Notice the stack grows *down,* not up.
POP	Pop word.	A = (SP) SP = SP + 2	
PUSHF	Push PSW.	SP = SP – 2 (SP) = PSW PSW = 0000H	Note that PUSHF clears the PSW after copying it into the stack. The effect is to disable all interrupts.
POPF	Pop PSW.	PSW = (SP) SP = SP + 2	

Shift Word Operations

Shift instructions have an 8-bit field, N, which indicates the number of places the word is to be shifted. If (N) $<$16, (N) is the shift count. If (N) $\geq$ 16, (N) is the address of the shift count. All shift operands must be in the Register File.

Mnemonic	*Meaning*	*Explanation/ Rules*
SHR	Shift right N places.	Each shift brings a 0 in from the left (into the MSB) and moves the LSB into C. The previous value of C is lost. If C loses any 1s during this series of shifts (except for the first shift), the ST bit (PSW.8) is set. Otherwise, ST = 0.
SHL	Shift left N places.	Each shift moves the MSB into C and a 0 in from the right (into the LSB). The previous value of C is lost. ST is unaffected.
SHRA	Shift right N places, with arithmetic sign.	Each shift brings a 0 (if the MSB is 0) or a 1 (if the MSB is 1) in from the left and moves the LSB into C. The previous value of C is lost. If C loses any 1s during this series of shifts (except for the first shift), the ST bit (PSW.8) is set. Otherwise, ST = 0. The shifted word has the same arithmetic sign as it did before the shift.

Byte and Double-Word Operations

A number of the previously described word instructions actually involve some byte and double-word variables, as well. For example, EXTB involves a byte operand, and MUL, MULU, DIV, DIVU, and EXT involve double-word operands. In addition, most of the arithmetic, logical, and data transfer instructions previously described for word operands have specifically byte versions, as listed below.

ARITHMETIC BYTE OPERATIONS

Mnemonic	*Meaning*	*Operation*	*Explanation/ Rules*
ADDB	Add 2 bytes.	D = D + A D = B + A	
ADDCB	Add with carry.	D = D + A + C	C is the carry bit (PSW.11).
SUBB	Subtract one byte from another.	D = D – A D = B – A	
SUBCB	Subtract with carry.	D = D – A – 1 + C	C is the carry bit (PSW. 11).
MULB	Multiply 2 bytes to form a double-byte (word) product.	D, D + 1 = D*A D, D + 1 = B*A	The address of the product must be a valid word address; that is, it must be even.
MULUB	Multiply unsigned.	D, D + 1 = D*A D, D + 1 = B*A	Same as MULB, except operands are treated as unsigned integers.
DIVB	Divide a word-integer by a byte-integer.	D = (D, D + 1)/ A D + 1 = remainder	The address of D must be a valid word address; that is, it must be even.
DIVUB	Divide unsigned.	D = (D, D + 1)/ A D + 1 = remainder	Same as DIVB, except operands are treated as unsigned integers.
INCB	Increment byte.	D = D + 1	
DECB	Decrement byte.	D = D – 1	
CMPB	Compare two bytes.	B – A	The result of the subtraction (B–A) is not stored. Only the PSW is affected.
NEGB	Negate byte.	D = –D	Changes the sign of the addressed byte.
EXTB	Extend byte to word.	D = D D + 1 = SIGN(D)	Sign–extends the addressed byte to word-length. (Hence the address of D must be a valid word address.)

LOGICAL BYTE OPERATIONS

Mnemonic	*Meaning*	*Operation*
ANDB	Logical AND.	D = D AND A D = B AND A
ORB	Logical OR.	D = D OR A
XORB	Exclusive OR.	D = D XOR A
NOTB	Logical NOT.	D = NOT(D)
CLRB	Clear byte.	D = 00H

DATA TRANSFER

Mnemonic	*Meaning*	*Operation*	*Explanation/ Rules*
LDB	Load byte.	D = A	Both operands are bytes.
STB	Store byte.	A = B	Both operands are bytes. In this case A, which can be anywhere in memory, is the destination register.
LDBSE	Load byte sign-extended to word.	D = A D + 1 = SIGN(A)	D is a word. A is a byte.

Mnemonic	*Meaning*	*Operation*	*Explanation/Rules*
LDBZE	Load byte zero-extended to word.	D = A D + 1 = 00H	D is a word. A is a byte.

Conspicuously absent from the byte-wide data transfer operations are PUSH and POP instructions. PUSH and POP are exclusively word operations. (Hence the Stack Pointer should *always* contain a valid word address, that is, it should be an even number.)

Byte and Double-Word Shift Operations

All of the word shift instructions have byte and double-word versions, as listed below. Their meanings and explanation are exactly the same as for the corresponding word shift instruction.

SHIFT OPERATIONS

Word	*Byte*	*Double-Word*
SHR	SHRB	SHRL
SHL	SHLB	SHLL
SHRA	SHRAB	SHRAL

There is one type of shift instruction that is exclusively for double-word operands:

Mnemonic	*Meaning*	*Explanation/Rules*
NORML	Normalize.	The (double-word) operand is left-shifted until the MSB is 1. The number of shifts required to do that is recorded in the Register File at a specified address. If the operand doesn't contain any 1s, the shifting will cease after 31 counts and the Z flag will be set.

Program Branching Instructions

UNCONDITIONAL JUMPS AND CALLS

Mnemonic	*Meaning*	*Explanation/Rules*
SJMP	Short jump.	Jump to an address that is within (+1023, –1024) of the current PC.
LJMP	Long jump.	Jump to an address that is within (+32767, –32768) of the current PC.
INDJMP	Indirect jump.	The instruction specifies a word address in the Register File. The PC is reloaded with the contents of that word.
SCALL	Short call.	Pushes the PC, then executes an SJMP to the subroutine. (Used when the subroutine is within (+1023, –1024) of the current PC.)
LCALL	Long call.	Pushes the PC, then executes an LJMP to the subroutine.
RET	Return.	Pops the PC, so that execution will continue from where it left off when the subroutine or interrupt service routine was branched to.

The 8096 assembler recognizes these mnemonics (except INDJMP), but also recognizes a number of generic jump and call instructions. For example, the assembler mnemonic BR (branch) translates to SJMP, LJMP, or INDJMP as required.

LOOP CONTROL

Mnemonic	Meaning	Explanation/Rules
DJNZ	Decrement and jump if not zero.	Instruction specifies a byte in the Register File which is to be decremented. If the result is not 00H, execution jumps to a specified address. The range is (+127, –128).

The normal application for DJNZ is as a loop counter, to control the number of times a program loop is executed.

CONDITIONAL JUMP INSTRUCTIONS

Conditional jump instructions test bits or combinations of bits to see if certain conditions are met. If they're met, the jump is executed. Otherwise execution continues in the normal sequence.

Most of these instructions test flag bits in the PSW. The flag bits involved are:

PSW.15	Z	Zero bit
PSW.14	N	Negative bit
PSW.13	V	Overflow bit
PSW.12	VT	Overflow trap bit
PSW.11	C	Carry bit
PSW.8	ST	Sticky bit

Mnemonic	*Meaning*	*Bit(s) Tested*	*Explanation*
JBS	Jump if bit set.	B.x	B is any byte in the Register File or SFR space. x is any bit in B. The jump is executed if B.x = 1.
JBC	Jump if bit clear.	B.x	Same as JBS, except the jump is executed if B.x = 0.
JC	Jump on carry.	C	Jump if C = 1.
JNC	Jump on no carry.	C	Jump if C = 0.
JE	Jump if equal.	Z	Jump if Z = 1.
JNE	Jump if not equal.	Z	Jump if Z = 0.
JGE	Jump if greater than or equal to.	N	Jump if N = 0.
JLT	Jump if less than.	N	Jump if N = 1.
JGT	Jump if greater than.	N, Z	Jump if N and Z are *both* 0.
JLE	Jump if less than or equal to.	N, Z	Jump if N = 1 or Z = 1.
JH	Jump if higher.	C, Z	An unsigned version of JGT. Jump if C = 1 and Z = 0.
JNH	Jump if not higher.	N, Z	An unsigned version of JLE. Jump if C = 0 or Z = 1.
JV	Jump on overflow.	V	Jump if V = 1.
JNV	Jump on no overflow.	V	Jump if V = 0.
JVT	Jump on overflow trap.	VT	Jump if VT = 1. Clear VT.
JNVT	Jump on no overflow trap.	VT	Jump if VT = 0. Clear VT.
JST	Jump on sticky bit.	ST	Jump if ST = 1.
JNST	Jump on no sticky bit.	ST	Jump if ST = 0.

The range of these jumps is limited to (+127, –128). The 8096 assembler, in addition to recognizing these mnemonics, also recognizes generic conditional jumps (such as BBS for JBS), in which the jump destination can range over the entire 64K.

SPECIAL CONTROL INSTRUCTIONS

Mnemonic	*Meaning*	*Explanation/ Rules*
SETC	Set carry bit.	
CLRC	Clear carry bit.	
CLRVT	Clear VT bit.	
DI	Disable interrupts.	Clears I (Interrupt bit, PSW.9). I = 0 disables all interrupts.
EI	Enable interrupts.	Sets I.
RST	Reset.	Activates the $\overline{\text{RST}}$ signal, triggering a reset.
NOP	No operation.	
SKIP	Skip.	Skips the next instruction byte. In effect, a two-byte NOP. The opcode for SKIP is 00H.

Notice the RST instruction. This instruction not only resets the CPU, but also activates the $\overline{\text{RST}}$ pin, so that external logic can also be reset. The opcode for the instruction was selected to be 0FFH, so that if a particularly harsh electrical transient (or a software error) causes the CPU to start executing nonimplemented memory, 0FFH will be read and the CPU will reset.

Addressing Modes

The addressing modes that are supported by the 8096 are as follows:

DIRECT

The operand is specified by an 8-bit address field in the instruction. The operand must be in the Register File or SFR space (locations 0000H through 00FFH).

IMMEDIATE

The operand itself follows the opcode in the instruction stream as immediate data. The immediate data can be either 8-bits or 16-bits, as required by the opcode.

INDIRECT

An 8-bit address field in the instruction gives the word address of a word register in the Register File which contains the 16-bit address of the operand. The operand can be anywhere in memory.

INDIRECT WITH AUTO-INCREMENT

Same as Indirect, except that, after the operand is referenced, the word register that contains the operand's address is incremented (by 1 if the operand is a byte, or by 2 if the operand is a word).

INDEXED

The instruction contains an 8-bit address field and either an 8-bit or a 16-bit displacement field. The 8-bit address field gives the word address of a word register in the Register File which contains a 16-bit base address. The 8- or 16-bit displacement field contains a signed displacement that will be added to the base address to produce the address of the operand. The operand can be anywhere in memory.

If the displacement field is 8 bits wide, the displacement value is sign-extended to 16 bits before being added to the base address.

The 8096 contains a Zero Register at word address 0000H (and which contains 0000H). This register is available for use as a base register in indexed addressing. This in effect provides direct addressing to all 64K of memory.

In the 8096, the Stack Pointer is at word address 0018H in the Register File. If the 8-bit address field contains 18H, the Stack Pointer becomes the base register. This allows direct accessing of variables in the stack.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias . . . . . 0° C to +70° C
Storage Temperature . . . . . -40° C to +150° C
Voltage from Any Pin to VSS or ANGND . . . -0.3V to +7.0V
Average Output Current from Any Pin . . . . . 10 mA
Power Dissipation . . . . . 1.5 Watts

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
TA	Ambient Temperature Under Bias	0	+70	C
VCC	Digital Supply Voltage	4.50	5.50	V
VREF	Analog Supply Voltage	4.95	5.05	V
fOSC	Oscillator Frequency	7.5	12	MHz
VPD	Power-Down Supply Voltage	4.50	5.50	V

VBB should be connected to ANGND through a 0.01 μF capacitor. ANGND and VSS should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
VIL	Input Low Voltage	-0.3	+0.8	V	
VIH	Input High Voltage	2.0	VCC+0.5	V	
VOL	Output Low Voltage		0.45	V	See Note 1.
VOH	Output High Voltage	2.4		V	See Note 2.
ICC	VCC Supply Current		200	mA	All outputs disconnected.
IPD	VPD Supply Current		1	mA	Normal operation and Power-Down.
IREF	VREF Supply Current		15	mA	
ILI	Input Leakage Current to all pins of HSI, P0, P3, P4, and to P2.1, P2.2, P2.3, and P2.4		±10	μA	Vin = 0 to VCC
IIH	Input High Current to $\overline{EA}$		100	μA	VIH = 2.4V
IIL	Input Low Current to all pins of P1, and to P2.6, P2.7, and READY		-100	μA	VIL = 0.45V
IIL1	Input Low Current to $\overline{RESET}$		-2	mA	VIL = 0.45V
Cs	Pin Capacitance (Any Pin to VSS)		10	pF	fTEST = 1MHz

NOTES:

1. IOL = 0.36 mA for all pins of P1, for P2.6 and P2.7, and for all pins of P3 and P4 when used as ports.

   IOL = 2.0 mA for TXD, RXD (in serial port mode 0), PWM, CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, and all pins of HSO and P3 and P4 when used as external memory bus (AD0-AD15).

2. IOH = -20 μA for all pins of P1, for P2.6 and P2.7.

   IOH = -50 μA for TXD, RXD (in serial port mode 0), PWM, CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, and all pins of HSO and P3 and P4 when used as external memory bus (AD0-AD15).

   P3 and P4, when used as ports, have open-drain outputs.

A/D CONVERTER SPECIFICATIONS

A/D Converter operation is verified only in devices having the "-A4" or "-A6" suffix.

The conversion accuracy is strongly dependent on the accuracy of VREF. The specifications given below assume adherence to the Operating Conditions section of these data sheets.

Resolution ..... ±0.001 VREF
Accuracy ..... ±0.004 VREF
Differential nonlinearity ..... ±0.002 VREF max
Integral nonlinearity ..... ±0.004 VREF max
Channel-to-channel matching ..... ±1 LSB
Crosstalk (DC to 100kHz) ..... -60dB max

AC CHARACTERISTICS

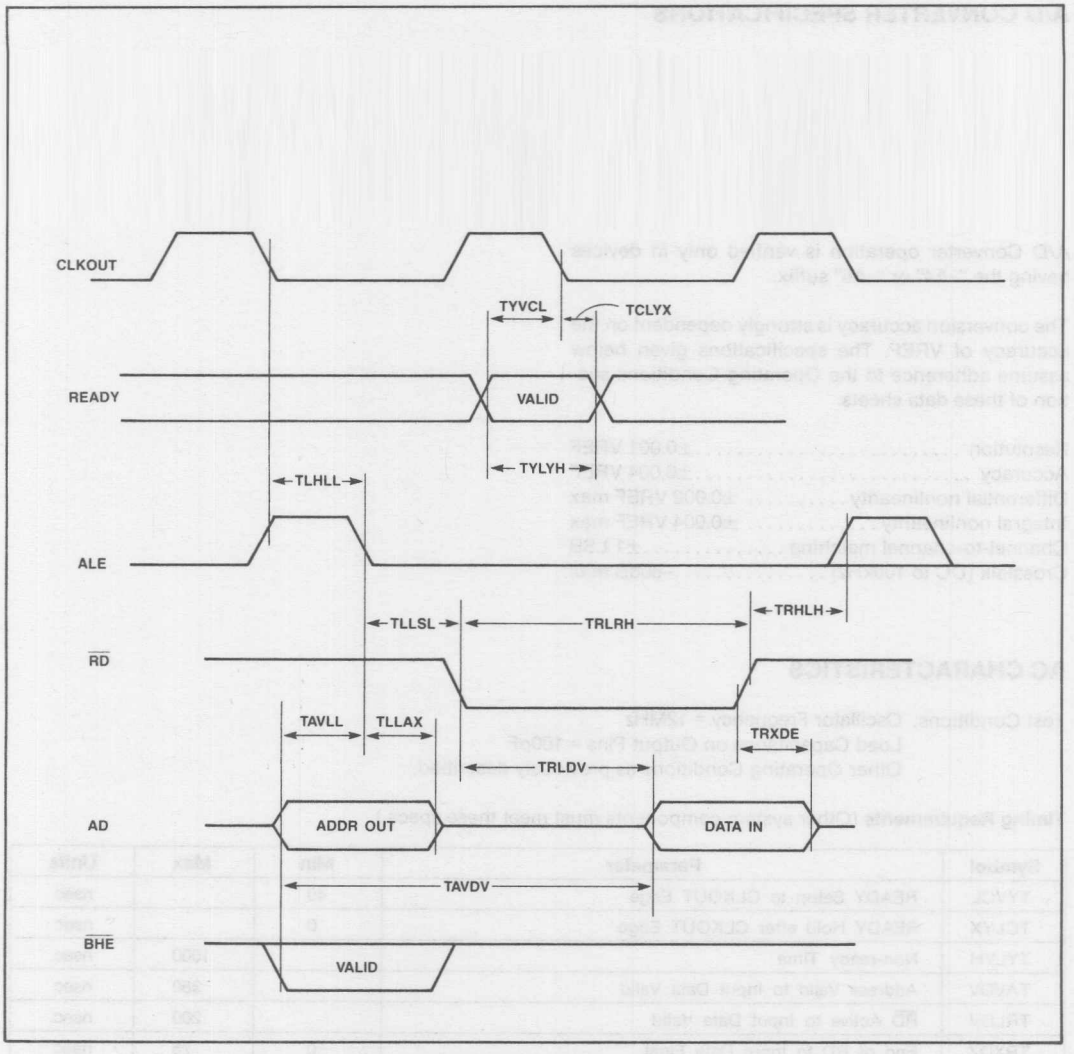
Test Conditions: Oscillator Frequency = 12MHz
Load Capacitance on Output Pins = 100pF
Other Operating Conditions as previously described.

Timing Requirements (Other system components must meet these specs.)

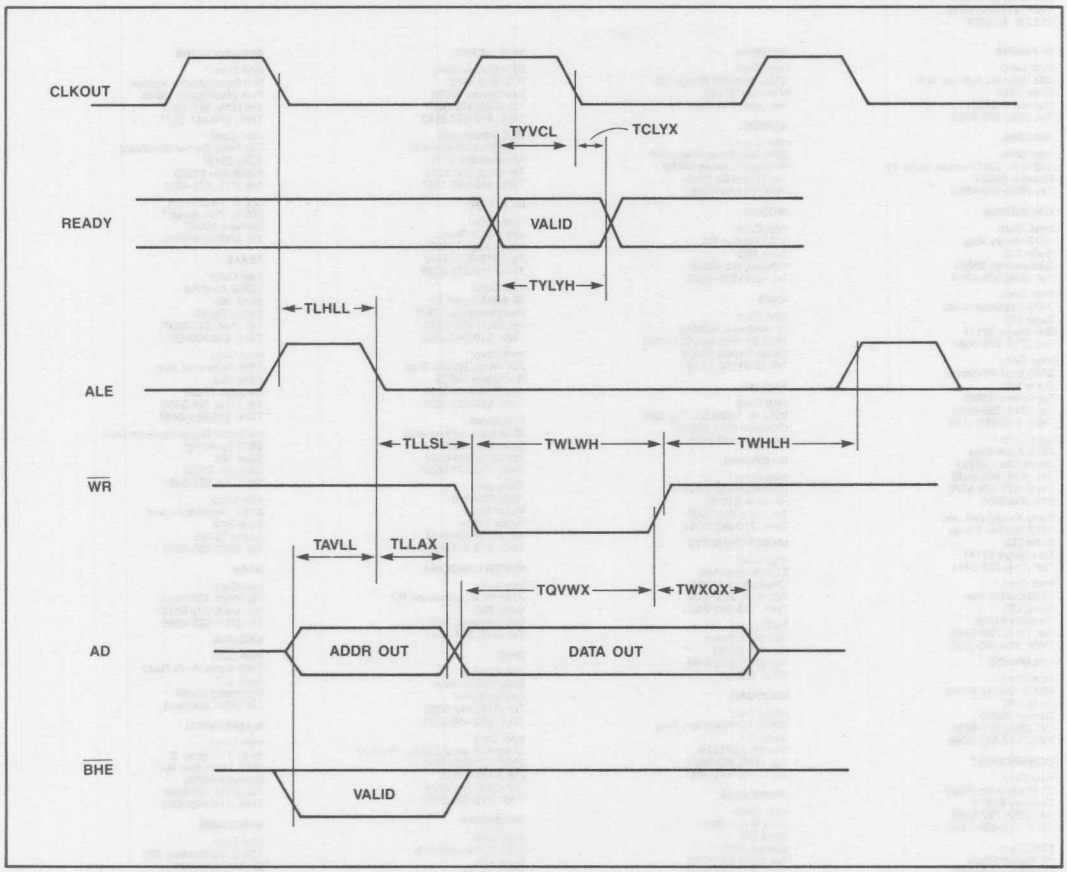
Symbol	Parameter	Min	Max	Units
TYVCL	READY Setup to CLKOUT Edge	40		nsec
TCLYX	READY Hold after CLKOUT Edge	0		nsec
TYLYH	Non-ready Time		1000	nsec
TAVDV	Address Valid to Input Data Valid		380	nsec
TRLDV	$\overline{RD}$ Active to Input Data Valid		200	nsec
TRXDZ	End of $\overline{RD}$ to Input Data Float	0	75	nsec

Timing Responses (iACX-96 meets these specs.)

Symbol	Parameter	Min	Max	Units
TLHLL	ALE Pulse Width	70		nsec
TAVLL	Address Valid to End of ALE	60		nsec
TLLSL	End of ALE to $\overline{RD}$ or $\overline{WR}$ Active	65		nsec
TLLAX	End of ALE to Address Invalid	65		nsec
TWLWH	$\overline{WR}$ Pulse Width	150		nsec
TQVWX	Output Data Valid to End of $\overline{WR}$	135		nsec
TWXQX	Output Data Hold after $\overline{WR}$	60		nsec
TWHLH	End of $\overline{WR}$ to Next ALE	140		nsec
TRLRH	$\overline{RD}$ Pulse Width	220		nsec
TRHLH	End of $\overline{RD}$ to Next ALE	75		nsec



External Memory Read Cycle



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